W601 Specification

V1.0.2

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Document History

Version	Date	Revision Record	Author	Approver	Auditor
V1.0.0	2019-2-20	Initial release	Ray		
V1.0.1	2019-3-6	Add 2MFlash discription	Ray		
V1.0.2	2019-5-17	Modify MCU&Wi-Fi function description	Ray		

Content

1 Features

- Chip Packaging
  - Package QFN68, 7mm x 7mm
- Chip Integration
  - MCU Function
    - Integrated 32bit Embedded Cortex-M3 CPU, operating frequency 80MHz; Integrated 288KB RAM and 1MB/2MB FLASH;
    - Integrated 8 channel 10bit differential ADC;
    - Integrated 1 master-slave SPI controller, with the operation frequency 20MHz;
    - Integrated 1 high speed slave SPI controller, max operating frequency 50MHz;
    - Integrated one I²C controller, support data transmission rate 100/400Kbps;
    - Integrated GPIO controller, support max 48 programmable GPIO;
    - Integrated 5 channel PWM;
    - Integrated I²S controller;
    - Integrated 7816 interface, support EVM2000 protocol and UART protocol;
    - Integrated LCD controller, support 8x16/4x20 interface, support 2.7V~3.6V output;
    - Integrated encrypted hardware accelerator, support PRNG, SHA1, MD5, RC4, DES, 3DES, AES, CRC.
  - Wi-Fi Function
    - Support GB15629.11-2006, IEEE802.11 b/g/n/;
    - Support Wi-Fi WMM /WMM-PS /WPA /WPA2 /WPS;
    - Support EDCA channel access;
    - Support 20/40M bandwidth;
    - Support STBC, Greenfield, Short-GI and reverse transmission;
    - Support AMPDU, AMSDU;
    - Support IEEE802.11n MCS 0~7, MCS32, transmission rate is up to 150Mbps;
    - Support Short Preamble in 2/5.5/11Mbps;
    - Support HT-immediate Compressed Block Ack, Normal Ack, No Ack;
    - Support CTS to self;
    - Support STA, AP, APSTA function.

2 General Description

Wi-Fi MCU W601 is a SoC chipset which support multiple interface and functions. It can be used as a master controller MCU and can be easily applied to smart appliances, smart home, health care, smart toy, wireless audio & video, industrial and other IoT fields.

3 Overview

This SoC integrates Cortex-M3 CPU, 1MB or 2MB Flash, RF Transceiver, CMOS PA, Baseband control. It applies multi interfaces such as SDIO, SPI, UART, GPIO, I²C, PWM, I²S, 7816, LCD, ADC etc. It applies multi encryption and decryption protocol such as PRNG, SHA1, MD5, RC4, DES, 3DES, AES, CRC etc.

4 Block Diagram

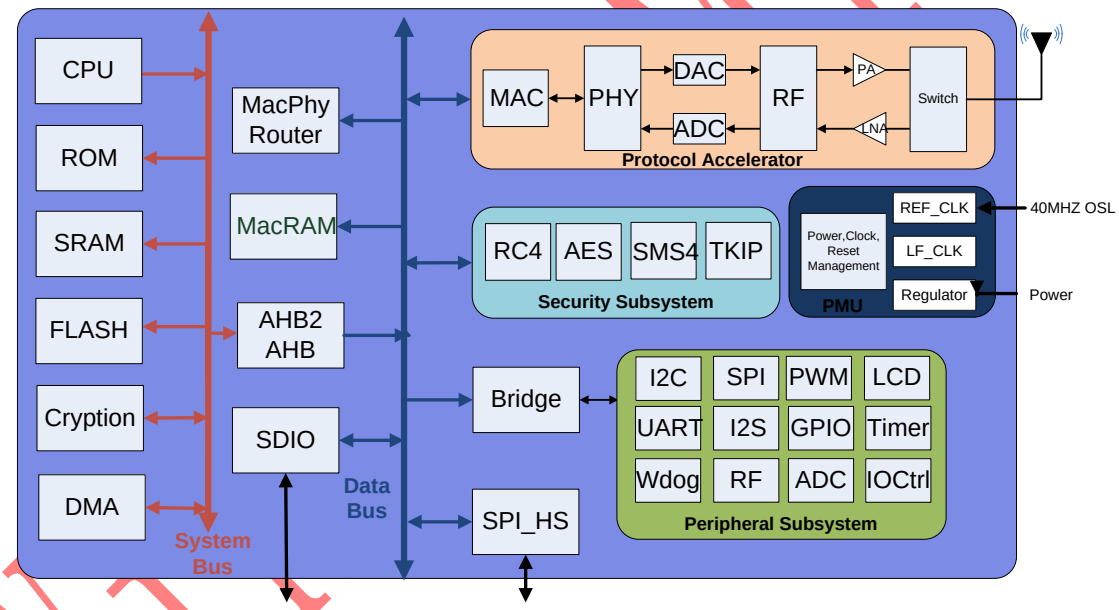

Figure4-1 W601 Block Diagram

5 Function Description

5.1 SDIO Controller

SDIO Controller transfer data with host and it has 1024 Bytes FIFO.

- Support SDIO2.0;
- Support frequency from 0 to 50MHz;

- Support block size up to 1024 bytes;
- Support soft reset;
- Support SPI, 1bit SD mode and 4 bits SD mode;

5.2 High speed SPI Controller

Support SPI protocol, has configurable data frame. The maximum data rate is 50Mbp.

- Support SPI protocol;
- Support alternative interrupt signal;
- Support max data rate 50Mbps;
- hardware decode and DMA data transfer;

5.3 DMA Controller

Support 8 channel, 16 DMA request signals, has chain table and register configuration.

- Support Amba2.0 protocol, 8 DMA channel;
- Support chain table operating mode;
- 16 configurable DMA request signals;
- Support 1,4-burst data transfer;
- Support byte-, half-word-, word- access;
- Programmable source or destination address unchanged, sequentially increases or pre-defined;
- Synchronous DMA request and DMA response timing;

5.4 Clock and Reset Controller

Support the control of clock and reset system. Clock control includes clock frequency conversion, clock turn off and adaptive gating, and reset control includes soft reset control of system and sub modules.

5.5 Memory Controller

Support the cache size configuration during transmitting and receiving, MAC access base address, cache number and frame aggregation control signals.

5.6 BBP

Support IEEE802.11a/b/g/e/n (1T1R). The main features are:

- Data rate: 1~54Mpbs (802.11a/b/g), 6.5~150Mbps (802.11n);
- MCS data format： MCS0~MCS7,MCS32(40MHz HT Duplicate mode);
- Support 40MHz bandwidth non-HT Duplicate mode, 6M～54M;
- Signal bandwidth： 20MHz, 40MHz;

- Modulation mode：DSSS(DBPSK,DQPSK,CCK) and OFDM(BPSK,QPSK,16QAM,64QAM);
- Support 1T1R MIMO-OFDM spatial multiplexing;
- Support Short GI mode;
- Support legacy mode and Mixed mode;
- Support data transmission and reception on 20M upper and low side in 40MHz bandwidth;
- Support STBC receive with MCS0～7, 32;
- Support Green Field;

5.7 MAC

Support IEEE802.11a/b/g/e/n MAC protocol. The main features of MAC are:

- Support EDCA channel access;
- Support CSMA/CA, NAV and TXOP;
- Support Beacon, Mng, VO, VI, BE, BK and QoS;
- Support unicast, broadcast and multicast;
- Support RTS/CTS,CTS2SELF,Normal ACK,No ACK frame format;
- Support retry and control of power and transmission rate;
- Support MPDU and Immediate BlockAck;
- Support RIFS,SIFS,AIFS;
- Support reverse transmission;
- Support programmable TSF Timer;
- Support MIB statistical information;

5.8 SEC

Support the security algorithm in IEEE802.11a/b/g/e/n protocol. Encryption or decryption in the process of transmitting and receiving data frames.

- Support throughput greater than 150Mbps;
- Support Amba2.0 bus protocol;
- Support WAPI2.0;
- Support WEP-64;
- Support WEP-128;
- Support TKIP;
- Support CCMP;

5.9 FLASH Controller

- Provide bus access in Flash interface;
- Provide arbitration between system bus and data bus;
- Implementation of CACHE;
- Support compatible with different QFlash;

5.10 RSA Encryption

RSA, arithmetic hardware coprocessor, provides Montgomery (FIOS) modular multiplication. The module implements of RSA algorithm with RSA software library, and supports from 128-bit to 2048-bit.

5.11 Encrypted Hardware Accelerator

The specified length data in the source address will be automatically en-/decrypted, and the result data will be write to the designated destination address space.

The module support PRNG (Pseudo random Number Generator), SHA1, MD5, RC4, DES, 3DES, AES, CRC.

5.12 I²C Controller

I²C Controller connects though APB Interface. Its supports master mode and configurable operating frequency （100K-400K）.

5.13 Master/Slave SPI Controller

Its support Master/Slave operating mode. The operating frequency is the frequency of system Bus. The main features of the bus are：

- Provides separate 8-level depth transmit and receive FIFO buffers;
- support Motorola SPI protocol,（CPOL,CPHA）, TI protocol, macrowire protocol in master mode;
- support Motorola SPI protocol（CPOL,CPHA）in slave mode;
- Support full duplex and half duplex;
- support data length up to 65535bit in master mode;
- support data transfer of any bit length in slave mode;
- 1/6 system clock frequency is max frequency of spi_clk in slave mode;

5.14 UART Controller

- Support APB bus protocol;
- Support Interrupt or polling;
- Support DMA, Separate receive/transmit 32 bytes entry FIFO buffer;
- Programmable baud rate;
- Programmable number of data bit, 5-8bit, and parity bit;
- Programmable stop bit, 1 or 2;
- Support auto flow control/flow control function;
- Support Break frame;
- Support interrupt of overrun, parity error, frame error, rx break frame;
- Up to 16-burst byte DMA data transfer;

5.15 GPIO Controller

Has 48-bit configurable GPIO, programmable input or output, configurable interrupt.
GPIOA and GPIOB have the same function with different base address.

5.16 Timer Controller

Configurable us or ms Timer, has 6 programmable 32-bit timers, Use interrupt flag to detect Time out.

5.17 Watchdog

The Watchdog is used to perform a system reset when system runs into an unknown state. The system software must respond to a periodic interruption, otherwise a hard reset will be generated.

5.18 RF Configurator

Support SPI bus protocol. The operating clock is system clock. The main features of the bus is：

- Provides separate 1-word depth transmit and receive FIFO buffers;

5.19 RF Transceiver

- The RF transceiver includes a power amplifier, a transmission channel, a receiving channel, a phase locked loop and a SPI, which changes the working state of the chip by the signals SHDN, RXEN and TXEN;
- The receiving channel uses the zero intermediate frequency structure to convert the RF signal directly to the baseband I and Q output. The RF front end works in 2.4GHz, including low noise amplifier and

orthogonal mixer. The baseband is composed of low pass filter and variable gain amplifier to realize channel filtering and gain control. The drive amplifier provides different DC output for the ADC interface.

- The transmission channel includes programmable control filter, upconverter mixer, variable gain amplifier and power amplifier. The transmission channel uses the output signal of direct frequency conversion structure. DAC signal through low pass filter, filter out the mirror frequency and out of band noise. PA output signal is differential output to drive antenna.

5.20 PWM Controller

- Has 5 PWM generators;
- Support 2 channels input capture (PWM0 and PWM4);
- Frequency range: 3Hz~160KHz;;
- Duty ratio precision: 1/256, Dead-Zone counter: 8bit;

5.21 I²S Controller

- Support AMBA APB bus protocol, 32bit single read/write;
- Operates as either Master or Slave, support full duplex;
- Capable of handling 8, 16, 24, 32 bits word size, sampling frequency is up to 128KHz;
- Support Mono and stereo audio data;
- Support I²S and MSB justified data format, support PCM A/B data format;
- Support DMA data transfer, word access only.

5.22 7816/UART Controller

- Support APB bus protocol;
- Support Interrupt or polling;
- Support DMA, Separate receive/transmit 32 bytes entry FIFO buffer;
- Support DMA data transfer, word access only. Up to 16-burst byte DMA data transfer;

Support UART and 7816 features：
UART features：

- Programmable baud rate;

- Programmable number of data bit, 5-8bit, and parity bit;
- Programmable stop bit, 1 or 2;
- Support auto flow control/flow control function (RTS/CTS);
- Support Break frame;
- Support interrupt of overrun, parity error, frame error, rx break frame;

7816 features:

- Support ISO-7816-3 T=0,T=1;
- Support EVM2000 protocol;
- Support guard time (11 ETU-267 ETU);
- Programmable inverse convention or direct convention;
- Support receive/transmit data frame with parity bit and retrans;
- Programmable stop bit, 0.5 or 1.5;

5.23 SAR ADC

This module is based on SAR ADC, support max 8 channel acquisition of analog signals, Sampling frequency is controlled by external input clock.

- Support max 8 channel data acquisition
- Support DMA module for data buffer. DMA operation is used with half word mode because ADC sampling data is half word
- Support interrupt interaction mode
- Support comparing function with sampling data and input data
- Before sampling data, the comparator misalignment calibration and Main DAC calibration are configurable
- Max sampling frequency is 10MHz

5.24 LCD Controller

- Support max 8COM x 16SEG or 4COM x 20SEG COM/SEG mode LCD
- Support Static, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8 duty mode
- Support Static, 1/2, 1/3, 1/4 bias Voltage
- LCD refresh frequency can be configured dynamically
- IO support 24mA driving capacity

- Support SPI interface character mode LCD

6 Pin Description

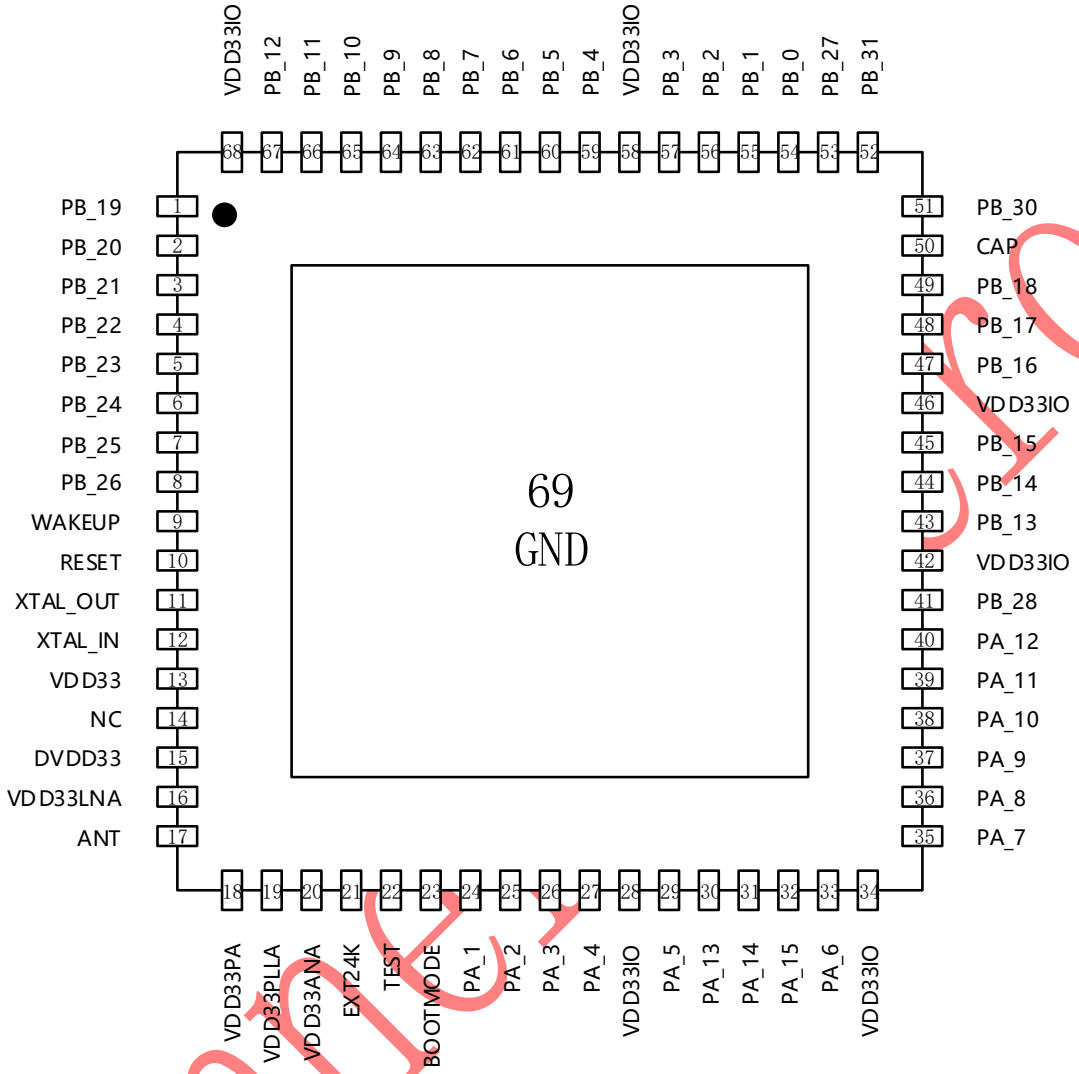

Figure 6-1 Pin Diagram (QFN68)

Table 6-1 Pin Description (QFN68)

Pin No.	Pin Name	Type	Function Description after reset	Multi-function
1	PB_19	I/O	PWM_0	UART2_RX, SAR-ADC1, GPIOPB_19
2	PB_20	I/O	PWM_1	UART2_TX, SIM_DATA, SAR-ADC2, GPIOPB_20
3	PB_21	I/O	PWM_2	UART2_RTS, SIM_CLK, I²C_SCL, SAR-ADC3, GPIOPB_21
4	PB_22	I/O	PWM_3	UART2_CTS, I²C_DAT, SAR-ADC4, GPIOPB_22
5	PB_23	I/O	PWM_4	UART0_CTS, SAR-ADC5, GPIOPB_23
6	PB_24	I/O	PWM_BREAK	UART0_RTS, SAR-ADC6, GPIOPB_24

7	PB_25	I/O	UART0_RX	SAR-ADC7, GPIOPB_25
8	PB_26	I/O	UART0_TX	SAR-ADC8, GPIOPB_26
9	WAKEUP	I	WAKEUP	
10	RESET	I	RESET	
11	XTAL_OUT	O	Output external crystal oscillator	
12	XTAL_IN	I	Input external crystal oscillator	
13	VDD33	P	Power supply, 3.3V	
14	NC		No use	
15	DVDD33	P	Power supply for digital circuit, 3.3V	
16	VDD33LNA	P	Power supply for LNA, 3.3V	
17	ANT	I/O	RF antenna	
18	VDD33PA	P	PA power supply, 3.3V	
19	VDD33PLLA	P	PLL power supply, 3.3V	
20	VDD33ANA	P	Power supply for analog circuit, 3.3V	
21	EXT24K	I	Series connect with a resistor to ground with 24KΩ+-1%	
22	TEST	I	Test mode	
23	BOOTMODE	I/O	BOOTMODE	UART2_RX, PWM_0, LCD_SEG0, GPIOPA_0
24	PA_1	I/O	UART2_TX	SIM_DATA, PWM_1, SPI(M/S)_CK, LCD_SEG1, GPIOPA_1
25	PA_2	I/O	UART2_RTS	SIM_CLK, PWM_2, SPI(M/S)_CS, I²S_M_MCLK, LCD_SEG2, GPIOPA_2
26	PA_3	I/O	UART2_CTS	PWM_3, SPI(M/S)_DI、I²S_M_SDA、LCD_SEG3、GPIOPA_3
27	PA_4	I/O	UART0_TX	PWM_4, SPI(M/S)_DO, I²S_M_SCL, LCD_SEG4, GPIOPA_4
28	VDD33IO	P	Power for IO, 3.3V	
29	PA_5	I/O	UART0_RX	PWM_0, SPI(M/S)_DI, I²S_M_EXTCLK, LCD_SEG5, GPIOPA_5
30	PA_13	I/O	UART0_RTS	I²S_M_RL, LCD_SEG6, GPIOPA_13
31	PA_14	I/O	UART0_CTS	I²S_S_SDA, LCD_SEG7, GPIOPA_14
32	PA_15	I/O	I²C_DAT	I²S_S_SCL, LCD_SEG8, GPIOPA_15
33	PA_6	I/O	I²C_SCL	I²S_S_RL, SDIO_CMD, LCD_SEG9, GPIOPA_6
34	VDD33IO	P	Power for IO, 3.3V	
35	PA_7	I/O	I²S_M_SDA	PWM_1, I²C_DAT, LCD_SEG10, GPIOPA_7

36	PA_8	I/O	I²S_M_SCL	PWM_2, UART0_TX, I²C_SCL, LCD_SEG11, GPIOPA_8
37	PA_9	I/O	I²S_M_RL	PWM_3, UART0_RX, SPI(M/S)-DO, LCD_SEG12, GPIOPA_9
38	PA_10	I/O	I²S_S_SDA	PWM_4, UART2_RX, SPI(M/S)-DI, LCD_SEG13, GPIOPA_10
39	PA_11	I/O	I²S_S_SCL	PWM_BREAK, UART2_TX, SIM_DATA, SPI(M/S)-CK, LCD_SEG14, GPIOPA_11
40	PA_12	I/O	I²S_S_RL	UART2_RTS, SIM_CLK, SPI(M/S)-CS, LCD_SEG15, GPIOPA_12
41	PB_28	I/O	I²S_M_MCLK	UART2_CTS, LCD_COM0, GPIOPB_28
42	VDD33IO	P	Power for IO, 3.3V	
43	PB_13	I/O	PWM_1	I²S_SCL, SDIO_CMD, GPIOPB_13
44	PB_14	I/O	H_SPI_INT	PWM_4, I²C_DAT, I²S_S_SDA, GPIOPB_14
45	PB_15	I/O	H_SPI_CS	PWM_3, SPI(M/S)_CS, I²S_S_SCL, GPIOPB_15
46	VDD33IO	P	Power for IO, 3.3V	
47	PB_16	I/O	H_SPI_CK	PWM_2, SPI(M/S)_CK, I²S_S_RL, GPIOPB_16
48	PB_17	I/O	H_SPI_DI	PWM_1, SPI(M/S)_DI, UART1_RX, GPIOPB_17
49	PB_18	I/O	H_SPI_DO	PWM_0, SPI(M/S)_DO, UART1_TX, GPIOPB_18
50	CAP	I	Capacitance, 1μF	
51	PB_30	I/O	UART2_RX	PWM_0, GPIOPB_30
52	PB_31	I/O	I²S_M_MCLK	GPIOPB_31
53	PB_27	I/O	SPI(M/S)-CK	LCD_COM1, GPIOPB_27
54	PB_0	I/O	SPI(M/S)-CS	UART2_CTS, PWM_BREAK, LCD_COM2, GPIOPB_0
55	PB_1	I/O	SPI(M/S)-DI	UART2_RTS, SIM_CLK, PWM_4, LCD_COM3, GPIOPB_1
56	PB_2	I/O	SPI(M/S)-DO	UART2_TX, SIM_DATA, PWM_3, LCD_COM4, GPIOPB_2
57	PB_3	I/O	JTAG_TRST	UART2_RX, PWM_2, I²S_S_SDA, LCD_COM5, GPIOPB_3
58	VDD33IO	P	Power for IO, 3.3V	
59	PB_4	I/O	JTAG_TDO	UART0_RTS, PWM_1, I²S_S_SCL, LCD_COM6, GPIOPB_4
60	PB_5	I/O	JTAG_TDI	UART0_CTS, PWM_0, I²S_S_RL, LCD_COM7, GPIOPB_5
61	PB_6	I/O	Reserved	SWDAT, UART0_RX, PWM_3, SIM_CLK, GPIOPB_6
62	PB_7	I/O	Reserved	SWCK, UART0_TX, SDIO_CMD, SPI(M/S)_CS, GPIOPB_7
63	PB_8	I/O	PWM_4	H_SPI_CK, SDIO_CK, I²S_M_SCL, GPIOPB_8

64	PB_9	I/O	UART1_CTS	H_SPI_INT, SDIO_DAT0, I²S_M_SDA, GPIOPB_9
65	PB_10	I/O	UART1_RTS	H_SPI_CS, SDIO_DAT1, I²S_M_RL, GPIOPB_10
66	PB_11	I/O	UART1_RX	H_SPI_DI, SDIO_DAT2, I²C_SCL, GPIOPB_11
67	PB_12	I/O	UART1_TX	H_SPI_DO, SDIO_DAT3, I²C_DAT, GPIOPB_12
68	VDD33IO	P	Power for IO, 3.3V	
69	GND	P	Ground	

1. I = input, O = output， P = Power

7 Parameters

7.1 Ultimate Characteristics

Table 8-1 ultimate characteristic

Parameter	Symbol	Min	Typ	Max	Unit
VDD supply voltage	VDD	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		VDD+0.3	V
Input capacitance	C_{pad}			2	pF
output low voltage	V_{OL}			0.4	V
output high voltage	V_{OH}	2.4			V
Max. output current	I_{MAX}			24	mA
Storage temperature	T_{STR}	-40℃		+125℃	℃
Operating temperature	T_{OPR}	-40℃		+85℃	℃

7.2 RF power parameters

Table 8-2 RF power parameters

Operation Mode	Typ	Unit
transmit IEEE802.11b, CCK 11Mbps, POUT = +19 dBm	230	mA
transmit IEEE802.11g, OFDM 54Mbps, POUT = +13.5 dBm	210	mA
transmit IEEE802.11n, OFDM MCS7, POUT = +12dBm	210	mA
receive IEEE802.11b/g/n	100-110	mA

7.3 Wi-Fi RF

Wi-Fi RF parameters

Parameter	Typ	Unit
Input frequency	2.4GHz~2.4835MHz	
Output Power		
72.2 Mbps PA Output Power	12	dBm
11b mode PA Output Power	19	dBm
Sensitivity		
DSSS, 1 Mbps	-95	dBm
CCK, 11 Mbps	-86	dBm
OFDM, 6 Mbps	-89	dBm

OFDM, 54 Mbps	-73	dBm
HT20, MCS0	-89	dBm
HT20, MCS7	-71	dBm
HT40, MCS0	-85	dBm
HT40, MCS7	-68	dBm
Adjacent Channel restrain		
OFDM, 6 Mbps	32	dB
OFDM, 54 Mbps	15	dB
HT20, MCS0	29	dB
HT20, MCS7	10	dB

8 Package Mechanical

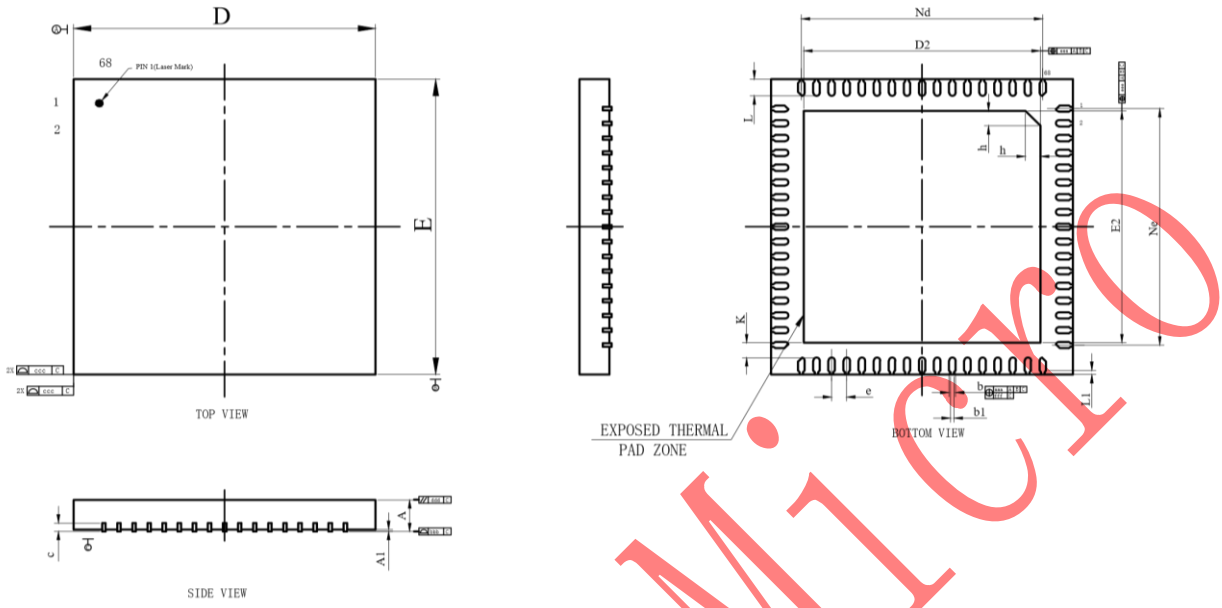

Figure 8-1 W601 package outline

Table 8-1 W601 package mechanical date

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.39	5.49	5.59
e	0.35BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.39	5.49	5.59
Ne	5.60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	--	--
h	0.30	0.35	0.40
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		
fff	0.05		
L/F (mil)	232*232		